

Predicting Operating Temperature and Expected Lifetime of Aluminum-Electrolytic Bus Capacitors with Thermal Modeling

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Abstract – Large-can aluminum electrolytic capacitors are widely used as bus capacitors in variable-speed drives, UPS systems and inverter power systems. Accurate thermal modeling of the capacitor’s internal temperature is needed to predict life, and this is a challenge because of the anisotropic nature of the capacitor winding and the complexity of the thermal coupling between the winding and the capacitor case. This paper translates analytical models for heat flow in bus capacitors into an equivalent three-loop, seven-resistor, lumped-parameter thermal circuit model. This paper presents the results of a Finite-Element Analysis (FEA)-based partial differential equation solution and the results of the three-loop thermal circuit model. The latter model is the basis for an operating temperature and expected lifetime Java applet which enables power-system designers to accurately predict capacitor operating temperature and expected life from operating conditions. Operating conditions permitted as inputs include applied voltage, ambient air temperature, air speed, thermal resistance of any heatsink attached, and capacitor characteristics like capacitance, ESR and case size.

I. INTRODUCTION

The useful life of an aluminum electrolytic capacitor is related to temperature exponentially, approximately doubling for each 10 °C the capacitor’s core temperature is reduced [1]. The temperature rise of the core is directly proportional to the core-to-ambient thermal resistance, and this paper models this thermal resistance for various capacitor construction techniques. Results are adapted for use in a new, lumped-parameter model suitable for use in a spreadsheet or a Java applet.

This paper focuses on modeling computergrade, or screw terminal, capacitors. However, the concepts can be applied to other aluminum electrolytic capacitor constructions, such as snapmount, radial, and axial capacitors.

An aluminum electrolytic capacitor is generally comprised of a cylindrical winding of aluminum anode and cathode foils separated by papers impregnated with a liquid electrolyte, usually based on ethylene glycol. See Fig. 1. The anode and cathode foils are made of aluminum, and the foils are usually highly etched. There is a thin coating of aluminum oxide on the surface of the anode. The anode and cathode foils are contacted by aluminum tabs that are extended from the winding. These tabs are attached to aluminum terminals in a polymeric top. The wet winding is sealed into an aluminum can.

Analytical and FEA models have been developed and recently published by one of the authors of the present paper, and the reader is referred to [2]. The present paper focuses on the embodiment of these models into a lumped-parameter circuit model and a corresponding Java applet.

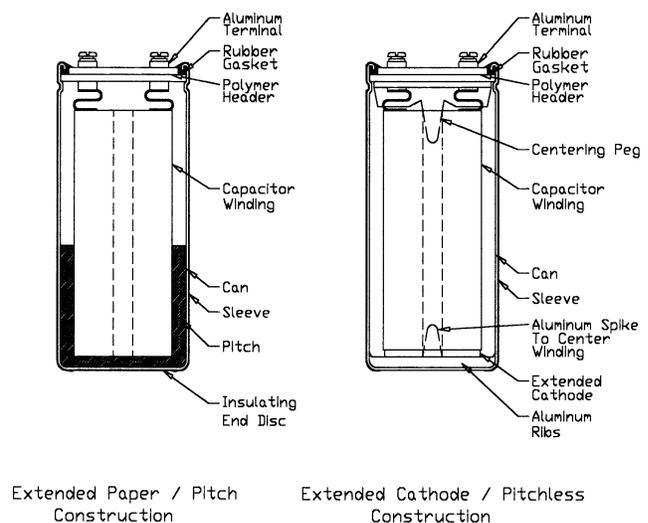


Fig. 1. Typical screw terminal capacitor constructions: pitch (left) and pitchless (right).

II. THE 7R THERMAL CIRCUIT MODEL

From recently developed thermal models [2] we find that the hot spot is generally in the top center of the winding. This hot spot is thermally isolated from the polymer top due to the low thermal conductivity of the top. The aluminum tabs have a high thermal conductivity, but due to their thin, narrow, and long dimensions, and the usual thermal isolation of the terminals, the tabs/terminals are generally not conducive to heat transfer. Thermal conduction within the winding occurs readily in the axial direction and somewhat less in the radial direction, due to the fact that the thermal conductivity is much larger in the axial direction than in the radial direction. This anisotropism occurs because the papers are effectively in parallel in the axial direction but in series in the radial direction, and the conductivity of the foil is nearly 1,000 times than that of the papers, even when the papers are wet with electrolyte.

The radial heat flow from the winding to the can is inhibited by a poor thermal path of either pitch or wet air. On the other hand, the axial thermal path from the bottom of the winding to the can bottom can be quite good, especially when an extended cathode construction is used instead of the more common wet paper and/or pitch. Therefore the principal heat flow is along the aluminum can from the capacitor bottom to the capacitor sides, and power is radiated and convected away from the capacitor bottom and sides to the environment.

A heatsink mounted to the bottom of the capacitor is an effective heat transfer mechanism since the lowest-resistance thermal path is axial. Extended cathode construction is a must when a heatsink is attached to the capacitor bottom in order to realize the advantage of the heatsink, because the primary thermal path is axial.

From the discussion thus far, it is apparent that there is an axial heatflow path, a radial path, and a coupling path via the capacitor can. This naturally leads to modeling the capacitor's thermal characteristics as a three-loop circuit. See Fig. 2a. Using an electrical circuit analogy, thermal power is analogous to electrical current, temperature is analogous to voltage, and thermal resistance is analogous to electrical resistance. See Fig. 2b.

Assuming that the two ambient temperatures and the seven thermal resistances are known, the value of the core temperature is determined as follows. We define

- R_1 = Thermal resistance, can bottom to heatsink/ambient
- R_2 = Thermal resistance, winding to can bottom
- R_3 = Axial thermal resistance of winding
- R_4 = Radial thermal resistance of winding
- R_5 = Thermal resistance, winding to can wall
- R_6 = Thermal resistance, can wall to ambient
- R_7 = Thermal resistance of can wall
- $R_A = R_2 + R_3$
- $R_B = R_4 + R_5$
- V_1 = Heatsink or ambient temperature ($^{\circ}\text{C}$)
- V_2 = Ambient temperature ($^{\circ}\text{C}$)
- V_3 = Temperature of can bottom ($^{\circ}\text{C}$)
- V_4 = Temperature of can side ($^{\circ}\text{C}$)
- V_C = Core temperature ($^{\circ}\text{C}$)
- I_S = Dissipated power (W)
- I_1 = Heat flow in loop 1 (W)
- I_2 = Heat flow in loop 2 (W)
- I_3 = Heat flow in loop 3 (W)

(1)

All resistance units are ($^{\circ}\text{C}/\text{W}$). Using Kirchoff's Voltage Law around Loop 1, we have

$$V_C = V_1 - I_1 R_1 - (I_1 - I_3) R_A, \quad (2)$$

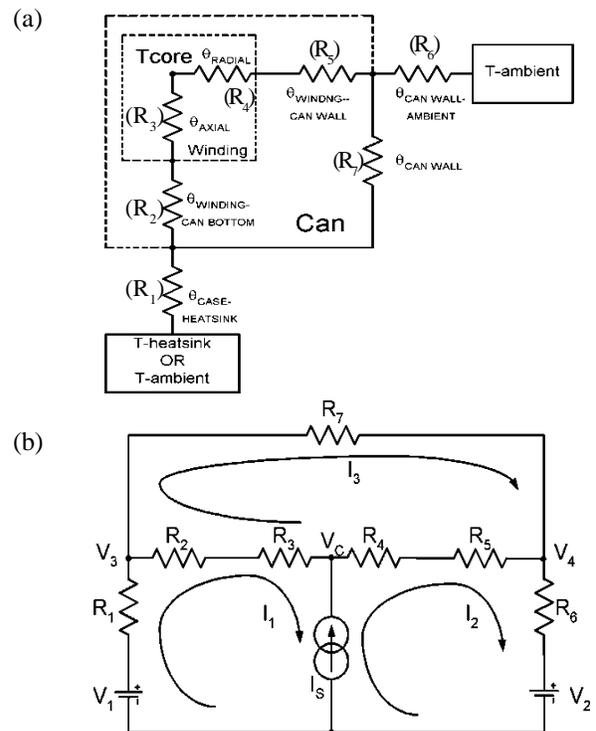


Fig. 2. (a,top) Thermal circuit equivalent for bus capacitor; (b,bottom) electrical circuit analogy.

and around Loop 2 we have

$$V_C = V_2 + I_2 R_6 - (I_2 - I_3) R_B . \quad (3)$$

Around the outer loop we obtain

$$V_1 = I_3 R_7 + I_1 R_1 + (V_2 + I_2 R_6) . \quad (4)$$

Equations (2), (3) and (4) may be combined to yield an expression relating I_3 to V_C in terms of known quantities as

$$I_3 = B V_C + C \quad (5)$$

where

$$B = \frac{\frac{R_1}{R_1 + R_A} - \frac{R_6}{R_6 + R_B}}{R_7 + \frac{R_1 R_A}{R_1 + R_A} + \frac{R_6 R_B}{R_6 + R_B}} \quad (6)$$

and

$$C = \frac{V_1 - V_2 - \frac{R_1 V_1}{R_1 + R_A} + \frac{R_6 V_2}{R_6 + R_B}}{R_7 + \frac{R_1 R_A}{R_1 + R_A} + \frac{R_6 R_B}{R_6 + R_B}} \quad (7)$$

Noting that $I_s = I_2 - I_1$, we may use (2) and (3) to obtain

$$I_s = E V_C + F . \quad (8)$$

where

$$E = \frac{R_6 + R_B + R_1 + R_A}{R_A(R_6 + R_B) - R_B(R_1 + R_A)} \quad (9)$$

and

$$F = \frac{I_s + \frac{V_1}{R_1 + R_A} + \frac{V_2}{R_6 + R_B}}{\frac{R_B}{R_6 + R_B} - \frac{R_A}{R_1 + R_A}} \quad (10)$$

Now (5) and (8) together yield

$$V_C = (F-C)/(B-E) , \quad (11)$$

which is the core temperature we seek.

III. THE THERMAL RESISTANCE VALUES

There are seven thermal resistances in this model as defined in (1). The value of the seven resistances may be calculated using the heat conduction equation and radiation/convection heat transfer theory along with the capacitor dimensions, effective thermal conductivities, and thermal properties of the environment. The necessary equations are presented in [2].

The thermal resistance, R_1 , from the can bottom to a heatsink or to the ambient, is either a conduction or a convection value, depending on whether the contact is to a metal plate or to air, respectively. For contact to a metal plate, R_1 is a contact resistance whose value is dictated by the clamping force, surface flatness, can bottom surface area A_{CB} [m²], and interfacial material properties. An approximate value for a conventional, sleeved capacitor is

$$R_{1COND} \approx 0.0059 / A_{CB} \quad [^{\circ}C/W]. \quad (12)$$

Adding a SilPad reduces this value by about 20%, while a bare aluminum can bottom clamped to a flat metal surface can reduce (12) by about 70%. The effective thermal resistance of a heatsink or chassis plate is derived in the next section.

For direct contact to moving air of velocity v [m/s], the convective thermal resistance is

$$R_{1CONV} = R_{1COND} + 1 / h A_{CB} \quad (13)$$

where h [W/m²K] is the combined convection/radiation coefficient [2]

$$h \approx 5 + 17 (v + 0.1)^{0.66} \quad (14)$$

The value of h increases slightly for small capacitors, varying as the negative one-fourth power of the diameter [3].

The thermal resistance R_2 from the capacitor winding to the capacitor bottom depends on the surface contact area A_w , the contact pressure, and the interface conductivity and thickness. For a tightly compressed screw terminal capacitor with wet paper or pitch providing the contact between the winding and the can bottom,

$$R_2 \approx 0.0075 / A_w \quad (15)$$

The coefficient indicated by (15) is reduced about 90% when extended cathode construction is used along with tight compression. This coefficient is also reduced somewhat in small-diameter capacitors and snapmount capacitors due to their narrower interface dimensions.

The axial thermal resistance R_3 of the capacitor winding is straightforward to calculate when the winding axial conductivity k_z (related to the relative foil and paper thicknesses) is known, along with the winding inner radius R_1 , winding outer radius R_o , and winding length L_w . Bearing in mind that the power is uniformly distributed, we have

$$R_3 \approx L_w / [2\pi k_z (R_o^2 - R_1^2)]. \quad (16)$$

The radial thermal resistance R_4 of the capacitor winding is also straightforward to calculate when the radial thermal conductivity k_r is known.

$$R_4 \approx [2R_1^2 \ln(R_o/R_1)/(R_o^2 - R_1^2) + 1] / (4\pi k_r L_w). \quad (17)$$

The radial thermal resistance R_5 from the capacitor winding to the can wall occurs via convection and radiation [2]. For an inner can diameter of D_c , an outer winding diameter of D_w , we have

$$R_5 \approx \ln(D_c/D_w) / (2\pi k_{RWC} L_w) \quad (18)$$

where k_{RWC} denotes the effective thermal conductivity in the region between the winding and the can wall. For pitch, $k_{RWC} \approx 0.2 - 0.3$ W/m·K.

For a vapor gap [2],

$$k_{RWC} \approx 0.030 + 0.65 \frac{\sigma D_w (T_w^4 - T_c^4) \ln(D_c/D_w)}{\left[\frac{1}{\epsilon_w} + \frac{1-\epsilon_c}{\epsilon_c} \left[\frac{D_w}{D_c} \right] \right] \Delta T} \quad (19)$$

where σ denotes the Stefan-Boltzmann constant, ϵ_w is the emissivity of the winding's outer surface, ϵ_c is the emissivity of the can's inner surface, T_w [K] is the winding surface temperature, T_c [K] is the can temperature, and $\Delta T = T_w - T_c$. Since T_w and T_c are not known, (19) requires that they be estimated. This estimation can

be done iteratively or by using other techniques.

The thermal resistance R_6 from the can wall to the ambient environment is obtained from

$$R_6 \approx 1 / hA_{CW} \quad (20)$$

where A_{CW} is the area of the can wall [m²] and h is given by (14).

Finally, the thermal resistance of the can wall is readily determined by heat conduction theory. This parameter should include the radial thermal resistance of the winding and can bottom as well as the axial thermal resistance of the can wall.

$$R_7 = R_4 // R_{CAN\ BOTTOM} + R_{SIDE} \quad (21)$$

where “//” indicates the parallel operation ($a/b = ab/(a+b)$) and

$$R_{CAN\ BOTTOM} \approx [2R_1^2 \ln(R_o/R_1)/(R_o^2 - R_1^2) + 1] / (4\pi k_{AL} d_b). \quad (22)$$

Here k_{AL} is the thermal conductivity of aluminum and d_b is the thickness of the can bottom. Also

$$R_{SIDE} = L / (4\pi k_{AL} R_c d_c) \quad (23)$$

where L is the can length, R_c is the effective can radius and d_c is the can wall thickness.

There are inherent limitations to the accuracy of the lumped parameter thermal model. First, some sources of error arise from the assumption that the can is at a constant temperature. We expect to make further refinements in estimating the effective average temperature of the can. Second, the contact resistances R_1 and R_2 vary with the contact force. Some capacitor designs have higher compression than others, and the width of the paper or cathode margin at the bottom of the winding varies from one design to another.

Verification of the vapor gap conductivity has been difficult, and we are still in the process of measuring the effect of can wall and winding emissivity variation experiments. Equation (19) provides winding-to-can-wall results that correlate with experimental data with $\epsilon_w = 0.85$ and $\epsilon_c = 0.40$.

IV. THERMAL RESISTANCE OF A CHASSIS PLATE

This discussion shows the effect of attaching the capacitor to a chassis plate for cooling. Generally the plate area is larger than that of the capacitor can, and there is some air movement and surface radiation. But the plate cannot usually be treated as an isothermal or even a constant-flux surface due to its appreciable conductance losses.

Consider a circular plate of radius R_p , thickness d_p , and thermal conductivity k_p , with a center-mounted capacitor of radius R_c dissipating power P into the plate, immersed in an environment (one side) of temperature T_A with combined radiation and convection coefficient h . The temperature distribution $T(r)$ may be found using the heat equation in cylindrical coordinates,

$$\frac{1}{r} \cdot \frac{d}{dr} \left[r \frac{dT}{dr} \right] + \frac{g}{k} = 0. \quad (24)$$

where g is the volumetric power density and r is the radial coordinate. We have two regions,

$$\frac{g}{k} = \begin{cases} -h(T - T_A) / (k_p d_p) & r > R_c \\ P / (\pi k_p d_p R_c^2) - h(T - T_A) / (k_p d_p) & r \leq R_c \end{cases} \quad (25)$$

Let us consider solutions in these two regions. First, for the outer region $r > R_c$ let

$$X_1 = T - T_A \quad r > R_c. \quad (26)$$

We have

$$\frac{d}{dr} \left[r \frac{dX_1}{dr} \right] - \frac{hX_1 r}{k_p d_p} = 0 \quad (27)$$

which expands to Bessel's equation

$$r \frac{d^2 X_1}{dr^2} + \frac{dX_1}{dr} - \frac{h}{k_p d_p} r X_1 = 0 \quad (28)$$

whose solution is [4]

$$X_1 = C_1 I_0(ar) + C_2 K_0(ar) \quad (29)$$

where

$$a = \sqrt{h / (k_p d_p)} \quad (30)$$

and $I_n(ar)$ and $K_n(ar)$ are modified Bessel functions of order n .

For the inner region $r \leq R_c$ let

$$X_2 = T - [T_A + P / (\pi k_p d_p R_c^2)] \quad r \leq R_c. \quad (31)$$

This leads to

$$X_2 = C_3 I_0(ar) + C_4 K_0(ar) \quad (32)$$

There are four constants, so that four boundary conditions are required. First, by symmetry we know that the heat flux at $r=0$ is zero so that

$$\left. \frac{dX_2}{dr} \right|_{r=0} = C_3 a I_1(0) - C_4 a K_1(0) = 0 \quad (33)$$

yielding $C_4 = 0$. We know that there is zero heat flux at the outer edge where $r = R_p$ so that

$$C_1 a I_1(aR_p) - C_2 a K_1(aR_p) = 0. \quad (34)$$

Hence

$$C_2 = C_1 \times I_1(aR_p) / K_1(aR_p). \quad (35)$$

We enforce temperature continuity at $r = R_c$ and obtain

$$(C_1 - C_3) I_0(aR_c) + C_2 K_0(aR_c) = P / (\pi R_c^2 h). \quad (36)$$

As the last boundary condition we apply Fourier's Law to the inward flux at $r = R_c$, assuming $T(R_c) \approx T(0)$ so

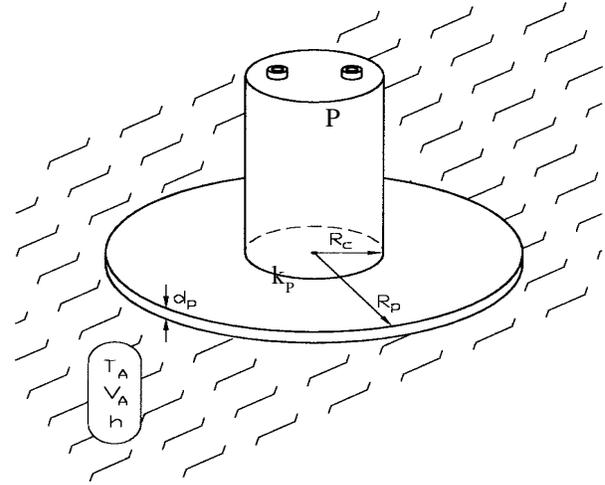


Fig. 3. Calculating the thermal resistance of a capacitor mounted to a chassis.

that

$$\left. \frac{dX}{dr} \right|_{r=R_c} = C_1 a I_1(aR_c) - C_2 a K_1(aR_c) \approx \frac{hR_c^2 X_1(R_c) - P}{2R_c k_p d_p} \quad (37)$$

We may solve equations (35), (36), and (37) simultaneously to obtain

$$C_1 = \frac{\frac{P}{2\pi R_c k_p d_p}}{\frac{aK_1(aR_c)}{K_1(aR_p)} + \frac{R_c h I_0(aR_c)}{2kt} + \frac{\pi R_c^2 h K_0(aR_c) I_1(aR_p)}{K_1(aR_p)} - a I_1(aR_c)} \quad (38)$$

$$C_2 = C_1 I_1(aR_p) / K_1(aR_p) \quad (39)$$

$$C_3 = C_1 + [C_2 K_0(aR_c) - P / (\pi R_c^2 h)] / I_0(aR_c) \quad (40)$$

Fig. 4 shows a typical temperature distribution plot. The effective thermal resistance from the capacitor bottom to the air may be found as

$$\theta_{CA} = (T(0) - T_A) / P. \quad (41)$$

In the example of Fig. 4, the chassis plate provides a thermal resistance of less than 1 °C/W to the ambient air, which would greatly reduce the core temperature and extend the life of the capacitor.

Air velocity =	800	lfm
Plate thickness =	0.0625	in
Plate conductivity =	250	W/mK
Cap diameter =	3	in
Power =	20	W
Ambient temperature =	45	°C
Plate diameter =	10	in

Temperature vs Radial Position

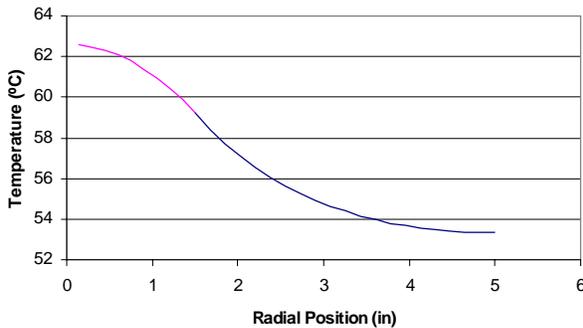


Fig. 4. Graph of the radial temperature distribution of a circular aluminum chassis plate with a center mounted capacitor.

V. TRANSIENT RESPONSE

So far we have discussed steady-state temperatures, but in many cases the capacitor core temperature response to a transient current surge or ambient temperature change needs to be evaluated. The thermal time constant τ of a capacitor is the time required for the core to reach 63% ($1 - e^{-1}$) of a step change in the ambient temperature. Once the effective thermal resistance from the core to the ambient is known, the thermal time constant of the capacitor may be calculated by lumped-parameter analysis if the Biot number Bi is much less than unity [5]:

$$Bi \equiv hL / k \ll 1. \quad (42)$$

Since per (14) the convection coefficient $h < 100$ W/m²K for air velocities less than 10 m/s, the winding length $L < 0.2$ m, and the axial winding conductivity $k_w \approx 100$ W/m-K [2], $Bi < 0.2$ and condition (42) is met for low and moderate air velocities and no heatsink. If $Bi > 0.2$ and a precise transient response is needed, FEA transient modeling techniques should be used. If $Bi < 0.2$,

$$\tau \approx m C_p \theta_{WA} \quad [s] \quad (43)$$

where m is the capacitor mass [kg], θ_{WA} is the thermal resistance from the winding to the ambient, and C_p is the specific heat [J/(kg·K)] of the winding, which we have measured to be approximately

$$C_p \approx 1400 \quad [J/(kg \cdot K)]. \quad (44)$$

The rate at which the core of a capacitor will heat when subjected to a power P , assuming an adiabatic process, where negligible heat energy transfer occurs over the period of interest, is therefore

$$dT_c/dt = P / (mC_p). \quad [°C/s] \quad (45)$$

Integrating (45), assuming the power P is applied at time $t=0$ and that the initial temperature is T_0 [°C], we obtain the core temperature response

$$T_c(t) = T_0 + P t / (mC_p). \quad (46)$$

This equation is useful for examining the effect of a high-current transient event. For example, if a capacitor is rated 10 amps rms but 40 amps rms is to be applied for one minute, (46) may be used to determine whether the capacitor will overheat. For extremely high current transients, other limitations such as tab fusing need to be addressed as well. Also, the capacitor mass m should be that of the winding only, excluding the pitch and other mass, when (45) with this lighter mass gives a thermal rise rate of greater than about 0.03 °C/s.

A capacitor's transient core temperature response to a step increase or decrease in ambient temperature ΔT is determined, subject to (42), by appealing to a DC electrical circuit model analogy. The model is of a capacitor transient voltage response to a DC voltage source being switched at $t=0$ to a series RC circuit. See Fig. 5. By inspection,

$$T_C(t) = T_0 + \Delta T [1 - \exp(-t / \tau)] \quad (47)$$

where T_0 is the initial capacitor and ambient temperature. Equation (47) is useful for examining the effects on the core temperature of brief exposure to a high ambient temperature such as in a wave-solder or solder-reflow machine. However, care must be taken to insure that the capacitor sleeve is not overheated, as splitting may occur.

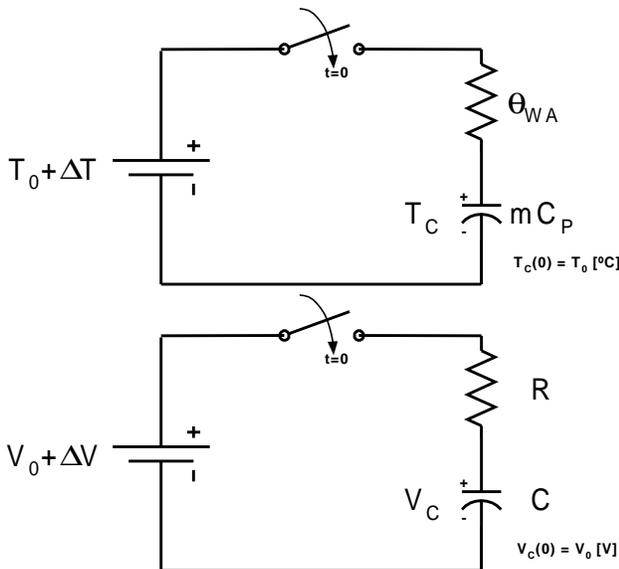


Fig. 5. (a,top) Transient thermal circuit equivalent for bus capacitor; (b,bottom) electrical circuit analogy.

VI. THERMAL MODEL RESULTS

Example output of an FEA-based partial differential equation solver is shown in Fig. 6. The accuracy of this model has been discussed and is usually within 10% [2]. Fig. 7 shows a comparison of results of the lumped-parameter “7R” thermal model presented in the present paper to some test data and to the FEA model.

VII. THE LIFE MODEL

The present life model that we use is based on test data and on life models used throughout the electrolytic capacitor industry. The model is based on the Arrhenius equation and on the activation energy of anodic aluminum oxide and the rate of decomposition of the electrolyte-spacer system. The life equation is used to model the approximate time interval at which the 85 °C effective series resistance (ESR) of a typical capacitor will exceed twice its initial value.

The life model that we use at present is

$$L = L_B \times M_V \times 2^{[(T_R - T_C)/10]} \quad (48)$$

where L_B is the base life in hours at the DC life test temperature at rated voltage V_R and rated temperature

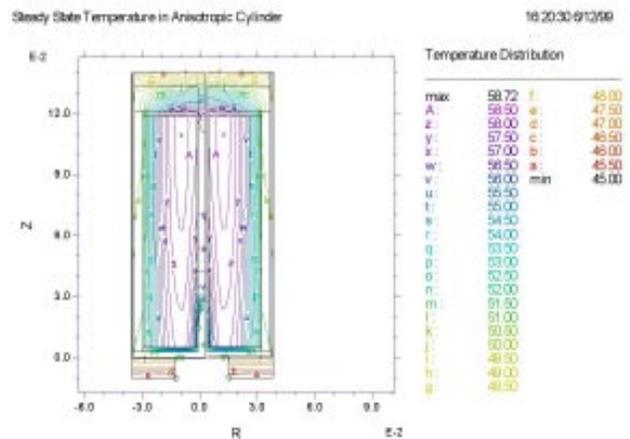


Fig. 6. Typical graphical output from FEA-based equation solver thermal simulation. This capacitor has extended cathode construction and is mounted to an annular heatsink with a thermal resistance of 1 °C/W.

T_R , T_C is the actual core temperature, and M_V is the DC voltage multiplier,

$$M_V = 4.3 - 3.3 \times V_A / V_R. \quad (49)$$

All voltages are in volts and temperatures in °C.

VIII. THE ESR MODEL

The effective series resistance (ESR or R_S) at 25 - 100°C is relatively straightforward to model. R_S contains a frequency-dependent dielectric loss R_{OX} due to the dissipation factor of the aluminum oxide dissipation factor, DF_{OX} , and a temperature-dependent loss R_{SP} due mostly to the electrolyte-impregnated paper and the liquid electrolyte in the etched pits or tunnels of the foil.

$$R_S = R_{OX} + R_{SP} \quad (50)$$

where

$$R_{OX}(f) = DF_{OX} / 2 \pi f C \quad (51)$$

and

$$R_{SP}(T) = R_{SP}(25^\circ\text{C}) \times 2^{A[-((T-25)/A)^B]} \quad (52)$$

$$25^\circ\text{C} \leq T \leq 100^\circ\text{C}$$

where the constants A and B are unique to the electrolyte-spacer system. Typical parametric values for a 400-

volts, ethylene glycol-based electrolyte-spacer system are $A = 40$ and $B = 0.6$.

A typical value for DF_{OX} is 0.015. Equation (51) can be refined by adding a slight positive temperature coefficient multiple to the DF_{OX} parameter.

It can be seen that the ESR has the largest magnitude at low temperature, low frequency, and that the ESR has the smallest magnitude at high temperature, high frequency. For a given capacitance and temperature, there is a frequency f_{FLAT} above which the additional ESR drop will be less than 10%:

$$f_{FLAT} \approx 5 DF_{OX} / (\pi R_{SP} C) \quad (53)$$

It is apparent that if the actual 25 °C, 120 Hz ESR and the DF_{OX} are known, that the ESR at all frequencies and temperatures above 25 °C can be found.

A few cautionary statements should be made concerning the use of this simple ESR model. When the ripple voltage

$$V_{RMS} \approx I_{RMS} / (2 \pi f C) \quad (54)$$

exceeds about 10% of the rated DC voltage, which can occur at low frequency, high ripple current, special capacitor design is required, and the heating and stability of a standard capacitor are often not well predicted by this simple ESR model.

Although R_S accounts for capacitor heating by modeling the capacitor losses as a series resistance, it should be noted that the dielectric loss accounted for by R_{OX} actually occurs inside the dielectric and does not cause a voltage drop at the capacitor terminals when a pulse current is applied.

For very low ESR capacitor designs ($R_S < 10$ milliohms) at $f > f_{FLAT}$, a term accounting for the foil and tab metal resistance should be added to (52) for enhanced accuracy. This term is relatively frequency and temperature invariant, and has an inverse relationship with the number of tabs.

At very high frequencies (above 50 kHz), the R_{SP} diminishes an additional 10-50% due to a transmission-line effect of the microscopic, electrolyte-filled, etched tunnels in the surface of the foil. The capacitance also decreases along with the R_{SP} , and together the roll-off occurs such that the tunnel impedance approaches a phase angle of -45°.

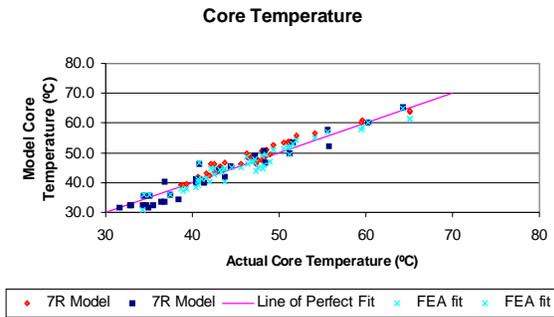


Fig. 7. Comparison of results from the 7R lumped-parameter thermal model and FEA-equation solver model versus test data. The test data includes capacitors in still air, isothermal heat sink, and moving air from 80 to 1000 LFM. Core rise above ambient was generally 10 - 30 °C. Capacitor sizes range from 1.375" diameter to 3.0" diameter.

IX. THE JAVA APPLET

The thermal, life, and impedance models presented in this paper have been combined and coded into a java applet to predict life. See Fig. 8. The inputs fields are selected or filled in as needed by the user. There is also a database search feature to locate a catalog capacitor if desired.

The seven resistances of the 7R thermal model are determined from the capacitor type (extended cathode or extended paper construction), winding size, and case size, as well as from the ambient parameters.

The 25 °C, 120 Hz ESR that the user has entered or that the database search feature has provided, along with the capacitor type, voltage rating, and capacitance, forms the basis for calculating $R_{sp}(25\text{ °C})$ and for establishing the ESR model for all frequencies and temperatures.

The prediction of the initial core temperature is found by calculating the power dissipation from the ESR model and the core temperature from the 7R thermal model. This is done iteratively because the dissipated power is a function of the ESR, the ESR is a function of the core

temperature, and the core temperature is a function of the power.

Analytical solutions to this problem generally include functions (such as the Lambert W function) that are not included in the math libraries of most spreadsheet and Java development packages. In the iterative solution of the java applet, the “seed” (initial guess) core temperature is set to the zero-power core temperature (usually the same as the ambient temperature), and the calculation loop usually settles to within 0.01 °C of the previous calculation within 10 iterations.

The calculated core temperature is the expected initial core temperature of the capacitor under the operating conditions specified by the user.

Since the ESR increases over the life of the capacitor, and the hot ESR is allowed to double, we base the life calculation on an “average” ESR that is 50% greater than the initial ESR. If the core temperature associated with this average ESR is greater than the maximum allowable core temperature, the user is alerted and life calculations are not presented.

X. CONCLUSIONS

In this paper we have developed a lumped parameter seven-resistor thermal circuit model whose resistances are based on the capacitor construction and relevant heat transfer theory. We have presented an ESR model and a life model. We have discussed the workings of a java applet that combines these three tools to predict core temperature and life.

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Fig. 8. Java Applet Life Calculator based on the 7R lumped-parameter thermal model, ESR model, and life model presented in this paper.